# Prosessor Arrays Design with the Use an Evolutionary Algorithm

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Nowadays the increasing interest of computations with the usage of a parallel architecture is observed. Presently there are a few the most popular platforms for parallel computations, like: supercomputers, multicore processors, graphical processor units and FPGA devices. Only the usage of FPGA platforms allows to adapt the platform architecture to the considered algorithm, although the knowledge of one of the hardware description languages HDL and designing experience are needed for the designing process to be effective. Presently there are a few translators from the C language to one of the HDL languages although the architectures obtained from this translators are not optimal. For the increasing effectiveness of the design process the whole functional blocks generators are used. The authors designed their own generator of accelerators for linear algebra algorithms dedicated for an implementation in FPGA devices.The design process of processor arrays consists in two steps. In the first the operations from the given algorithm are mapped to the processor element(alocation mapping). In the second step the realization time for each operation is calculated. The authors propose the usage of the evolutionary algorithm for allocation mapping and optimization of the runtime of the whole given algorithm. Presently there are a few described methods for processor arrays design but only the method proposed allows to exactly define the structure of a parallel architecture. In preliminary experiments the allocation mapping was computed for algorithms with small input matrices. For bigger matrices the authors could not obtain permissible space projection solutions. For this reason the authors decided to use the information dependencies graph decomposition in allocation mapping process. In the method proposed the solution grows up during the runtime of the designed method. The evolutionary algorithm operators worked in the assumed limits of a position in a chromosome. In this paper the authors present the allocation mapping with and without the information dependences graph decomposition. The authors also designed the parallel evolutionary algorithm which allowed to obtain the better results for short assumed design runtime.