Modeling Thermal Effects in Fully-Depleted SOI Devices with Arbitrary Crystallographic Orientation

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To achieve further improvement of performance in scaled silicon devices applied mechanical stress, alternative wafer orientations, and multi-gate transistors have been actively researched or are already in production. All these options take advantage of the anisotropic nature of the silicon crystal, and therefore, of its anisotropic bandstructure, in engineering gains in the carrier transport mass and mobility. For instance, strained Si is the only new channel material which has recently made its way into the commercial integrated circuits. By straining the silicon channel, carrier mobility can be enhanced. Also, devices fabricated on Si (110) wafer orientations has shown improved mobility characteristics over (100) devices.

The current trend in device scaling is a transition away from conventional planar CMOS to alternative non-planar technology devices, such as fully-depleted (FD), dual-gate (DG), tri-gate silicon-on-insulator (SOI) and others. The problem with SOI devices is that they exhibit self-heating effects. These self-heating effects arise from the fact that the underlying SiO2 layer has about 100 times smaller thermal conductivity than bulk Si. We have previously reported that self-heating and increased power density play important roles in the operation of fully-depleted SOI devices with channel lengths between 25 and 180 nm using 2D electro-thermal simulation based on the self-consistent solution of the Boltzmann transport equation for the electrons via Monte Carlo techniques and the energy balance equations for acoustic and optical phonons. There it was shown that due to geometry and velocity overshoot, self-heating effects are more pronounced for larger channel length devices with correspondingly larger supply voltages.

In this work we continue our investigation on the impact of the wafer crystallographic orientation on the current degradation in nanoscale FD-SOI devices due to self-heating effects. The preliminary results obtained from the simulated 25nm channel length FD-SOI structure show that the isothermal value of the on-current for (110) wafer orientation (ID=1.904mA/um for VGS=VDS=1.2V) is higher compared to the (100) wafer orientation (ID=1.772mA/um for VGS=VDS=1.2V). What is more important, the current degradation due to self-heating is slightly lower for (110) wafer orientation (2.6% versus 3.7% for (100)). From the lattice temperature profile, one can observe that the position of the hot-spot region doesnt change with the wafer orientation, but the maximum temperature is higher for (100) wafer orientation. These results are obtained by using our novel theoretical model for the temperature and thickness dependence of the thermal conductivity which is valid for (100) wafer orientation. We believe that the inclusion of the proper thermal conductivity model for (110) wafer orientation will decrease the current degradation even more. The results of these simulations will be presented at the conference.